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EXAMINER	
STEELMAN, MARY J	

ART UNIT	PAPER NUMBER
2122	

DATE MAILED: 08/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/976,286	MERIBOUT, MAHMOUD	
	Examiner	Art Unit	
	Mary J. Steelman	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/15/01, 6/17/02*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 June 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 are pending.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

3. Delete the reference numbers from the Abstract.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 13, 14, 15, 20, 21, and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent 5,966,534 to Cooke et al.

Cook disclosed:

Per claim 1:

A compiling method including:

-a first step of carrying out a syntax analysis of a description file describing a desired electronic circuit model with a predetermined high level description language, to generate a control data flow graph having a predetermined graph structure;

(Col. 2, lines 23-25, "A computer program, written in a high level programming language, is compiled into a n intermediate data structure which represents its control and data flow (control flow graph), col. 2, lines 60-63, "The computer program source code is parsed with standard

compiler technology into a language independent intermediate format. The intermediate format is a standard control and data flow graph, but with addition of constructs..."

-a second step of dividing said control data flow graph into threads composed of a set of a plurality of connected nodes and achieving a particular function, and optimizing the divided threads to meet with a predetermined area restriction and a predetermined waiting time restriction, to obtain designation information of the number, the function, the placement and routing of logic cells for the desired electronic circuit model.

(Col. 5, lines 14-16, "...two runtime parameters: the maximum area for a single ASIC block and the maximum total ASIC area..." ,col. 5, lines 65-67, "Traversing the list by increasing finish times, each function is assigned to the same FPGA block until the FPGA block's area capacity is reached...", col. 6, lines 20-27, "In list scheduling...Each node in the task graph is assigned a priority...Tasks are sorted in decreasing order of task priorities."

Per claim 13:

-said electronic circuit model is constituted of a hardware cell formed of a predetermined number of basic elements.

Col. 3, line 18-20, "...our methodology uniquely supports code generation for two different types of target hardware: standard microprocessor and ASIC", col. 5, line 34, 'FPGA', col. 5, line 36, 'reconfigurable'.

Per claim 14:

-hardware cell is one of an application specific integrated circuit, a field programmable gate array and a dynamic reconfigurable logic.

Col. 3, line 18-20, "...our methodology uniquely supports code generation for two different types of target hardware: standard microprocessor and ASIC", col. 5, line 34, 'FPGA', col. 5, line 36, 'reconfigurable'.

Per claim 15:

A synthesizing system including:

-a front-end compiler means for carrying out a syntax analysis of a description file describing a desired electronic circuit model with a predetermined high level description language, to generate a control data flow graph having a predetermined graph structure;

-a back-end compiler means for dividing the control data flow graph into threads composed of a set of a plurality of connected nodes and achieving a particular function, and optimizing the divided threads to meet with a predetermined area restriction and a predetermined waiting time restriction, to obtain designation information of the number, the function, the placement and routing of logic cells for the desired electronic circuit model.

(See limitations as addressed in claim 1 above.)

Per claim 20:

-said electronic circuit model is constituted of a hardware cell formed of a predetermined number of basic elements.

(See limitations as addressed in claim 13 above.)

Per claim 21:

-said hardware cell is one of an application specific integrated circuit, a field programmable gate array and a dynamic reconfigurable logic.

(See limitations as addressed in claim 14 above.)

Per claim 22:

A recording medium recording a computer program for causing a computer to execute a processing for carrying out a syntax analysis of a description file describing a desired electronic circuit model with a predetermined high level description language, to generate a control data flow graph having a predetermined graph structure, and another processing for dividing the control data flow graph into threads composed of a set of a plurality of connected nodes and achieving a particular function, and optimizing the divided threads to meet with a predetermined area restriction and a predetermined waiting time restrictions to obtain designation information of the number, the function, the placement and routing of logic cells for the desired electronic circuit model.

(See limitations as addressed in claim 1 above.)

Claim Rejections - 35 USC § 103

5. Claims 2-12 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 5,966,534 to Cooke et al.

Per claim 2:

-the optimization in said second step is carried out by estimating a minimum boundary of an area and a waiting time in connection with any of a function unit, a register and a multiplexer.

Cooke disclosed syntax analysis used to optimize design of an electronic circuit model. Cooke disclosed area and time considerations. Col. 5, line 14, "two runtime parameters: the maximum area...", col. 5, lines 54-54, "...minimize the overall execution schedule (time)...", in connection with any of a function unit, a register... col. 4, line 6, "...register..."

Cooke failed to disclose details regarding a minimum boundary of an area, but did consider that area should be sufficient. Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention to modify Cooke's invention to include estimations of a minimum boundary of an area when developing a syntax analysis of a description file because it is an important element to consider when searching for an optimal design.

Per claim 3:

-the optimization in said second step is carried out by first optimizing the divided threads to meet with the predetermined area restriction, and thereafter optimizing the optimized threads to meet with the predetermined waiting time restriction.

Cooke disclosed at col. 3, lines 64-66, "One implementation passes the intermediate control and data flow graphs to a behavioral synthesis program." Various steps are processed in

the optimization of the threads. Area and time restrictions are considered. Col. 4, lines 58-61, To determine the amount of ASIC area required to implement a source code loop...", col. 5, lines 52-55, "The various functions comprising a snapshot are partitioned into separate blocks by the compiler in order to minimize the blocks stall time..." Cooke failed to specify steps and the order of steps, however, both time and area are considerations of the optimal solution and thus would be obvious.

Per claim 4:

-said second step includes:

-a top-down processing step carrying out the optimization in connection with the predetermined area restriction and the predetermined waiting time restriction, in the order from a highest level divided thread;

Cooke disclosed, col. 5, lines 65-67, "Traversing the list by increasing finish times, each function is assigned to the same FPGA block until the FPGA block's area capacity is reached.", col. 6, lines 1-10, "After all functions have been assigned to FPGA blocks, we calculate for each FPGA block the difference between the earliest and the latest finish times (predetermined waiting time restrictions)"

-a down-top processing step of dividing a lower level divided thread optimized in said top-down processing step, into some number of threads, to assemble into a predetermined context or a predetermined circuit.

Cooke disclosed dividing the threads to further optimize, col. 6, lines 42-45, "program may be divided into more than one section, where the total number of configurations for any FPGA block does not exceed the capacity…

While not specifically disclosing, "in the order from a highest level divided thread" and dividing in a "top-down processing step", Cooke did disclose time and area considerations and subdividing the threads to obtain a better optimization.

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention to modify Cooke's invention to include an algorithm of top-down processing from a highest level thread, because it is a logical manner to approach thread optimization.

Per claim 5:

-top-down processing step includes:

Col. 2, lines 52-64.

-a first dividing step for dividing the control data flow graph into threads composed of a set of the plurality of connected nodes and achieving the particular function;

Col. 2, line 28-30.

-a first scheduling step of allocating a predetermined control step and a thread moving range in that step for a thread obtained in the first dividing step, the first scheduling step also allocating the order of priority for the threads respectively allocated with the control steps, in accordance with a plurality of priority order lists previously set;

Col. 5, line 59-62.

-a first area restriction determining step for estimating a total area of the threads allocated in the first scheduling step, and of determining whether or not the estimated total area meets with the predetermined area restriction;

Col. 5, lines 65-67.

-when it is determined in the first area restriction determining step that the estimated total area does not meet with the predetermined area restriction, a similarity cost calculating step for calculating a similarity cost in connection with an area for all thread pair combinations of the threads obtained in the first dividing step;

Col. 6, lines 5-8.

-a first allocation step of selecting, from the thread pairs, a thread pair belonging to different control steps and having a further high similarity cost, with reference to the similarity costs obtained in the similarity cost calculating step, the first allocation step further obtaining a new thread by combining the selected thread pair as a new thread to another thread;

Col. 6, lines 9-18.

-a second area restriction determining step for estimating a total area for the new thread pair obtained in the first allocation step, and of determining whether or not the estimated total area meets with the predetermined area restriction;

Col. 6, lines 9-18.

-when it is determined in the second area restriction determining step that the estimated total area does not meet with the predetermined area restriction, an allocation-scheduling step of selecting, from the threads included in the list, a thread pair belonging to the same control step and

having a further high similarity cost, in accordance with the plurality of priority order lists, in the order from a low priority list, the allocation-scheduling step obtaining a new thread pair by combining the selected thread pair as a new thread to another thread, and subdividing the control step allocated to the new thread pair, into two control steps having the same content;

Col. 6, lines 45-48.

-when it is determined in the first or second area restriction determining step that the estimated total area meets with the predetermined area restriction, a thread processing step of investigating a trade-off between the area restriction and the waiting time restriction for the new thread pair obtained in the first allocation step or in the allocation-scheduling step, and carrying out the placement and routing of nodes to meet with both the restrictions;

Col. 6, line 56-58.

-wherein said down-top processing step includes:

-a second scheduling step of selecting and separating, for the threads placed and routed in the thread processing step, a thread pair having a low similarity, from the threads included in the list, in accordance with the plurality of priority order list, in the order from a high priority list;

Col. 6, lines 42-44.

-a second dividing step of assembling the thread pairs separated in the second scheduling step, into a context or a circuit which minimizes a connecting restriction between threads.

Col. 6, lines 42-44.

While Cooke disclosed processing a control data flow graph, by dividing into threads, and optimizing, using time and area considerations, grouping and re-grouping thread pairs, he

did not specifically disclose the claim limitations algorithm as recited in claim 5. Cooke did not specifically "provide for a cost calculating step calculating a similarity cost in connection with an area for all thread pair combinations", "selecting a thread pair belonging to different control steps and having a further high similarity cost".

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention to have included steps to consider "similarity costs" when deciding between thread pair combinations, because Cooke was considering time and area in finding an optimal solution and suggested regrouping threads to achieve this.

Per claim 6:

-the predetermined time restriction in said thread processing step includes three restrictions, a movement range restriction defined as a movement range of the thread in said control step, a thread sharing restriction defined as an overlapping in time between the threads in said control step, and a pipeline restriction defined as a waiting time for the thread belonging to one loop of a pipeline processing executing said control step in parallel.

Col. 7, lines 20-27. Cooke provided suggestion for time considerations when optimizing compilation of a high level programming language into an integrated processor and thus would be obvious.

Per claim 7:

-thread processing step includes:

-when new thread pairs obtained in said first allocation step or said allocation-scheduling step include a thread pair which does not meet with one of said movement range restriction, said thread sharing restriction and said pipeline restriction, a thread adjusting step for finding out a solution having a minimum thread area meeting with those restrictions for said thread pair;

Col. 6, lines 42-45, "program may be divided..."

-a thread optimizing step for investigating a critical path having a maximum delay, for a thread pair obtained in said thread adjusting step, on the basis of a predetermined connectivity restriction, to assemble nodes into a cluster, when there exists a thread having a waiting time longer than a predetermined clock cycle, said thread optimizing step obtaining the number of registers to be inserted into said thread, and estimating a minimum area by timing said registers, thereby to obtain a solution meeting with said predetermined waiting time restriction.

Col. 2, line 26, "...identify critical blocks of logic...", col. 5, lines 52-55, "The various functions comprising a snapshot are partitioned into the separate blocks...", col. 6, lines 14-18, "The setoff all such configuration tasks across all snapshots may be scheduled...".

Cooke failed to specifically disclose "with one of said movement range restriction, said thread sharing restriction and said pipeline restriction, a thread adjusting step for finding out a solution having a minimum thread area meeting with those restrictions for said thread pair", "optimizing step obtaining the number of registers to be inserted into said thread, and estimating a minimum area by timing said registers, thereby to obtain a solution", but he did consider time, area and resources when attempting to obtain an optimal solution and thus it would have been obvious.

Per claim 8:

-thread processing step includes;

-a step of calculating a closeness matrix representing the closeness of nodes of each thread for the thread pair obtained in said thread adjusting step;

Col. 5, line 52-58.

-a step for generating a node cluster tree by grouping nodes based on said closeness matrix;

Col. 5, lines 59-62.

-a step for investigating a critical path having a maximum delay on the basis of the connectivity metrics of each node pair in said node cluster tree;

Col. 2, lines 28-30.

-a step of grouping said node pairs included in said node cluster tree on the basis of whether or not the node pair belongs to said critical path, thereby to constitute an elementary block, and further grouping elementary blocks closest to each other, to constitute a macro block.

Col. 5, lines 52-55, col. 5, line 65-col. 6, line 18, col. 2, lines 30-33.

While Cooke disclosed analysis of a flow graph to choose groups of nodes, he did not specifically disclose a "closeness matrix" when determining a thread pair.

However, it would have been obvious, because Cooke was traversing the tree to choose optimal thread pairs and therefore searching nodes that are close to each other when traversing a critical path. Thus a concept of "closeness" is obvious.

Per claim 9:

-said thread adjusting step and in said thread optimizing step, the step for finding out the solution is carried out by connecting a library supplying a set of function units which have corresponding area and delay and which have a predetermined parameter which can be set.

Col. 4, lines 4-6, "...library of circuit implementations...", col. 5, line 24, "...apply the knapsack algorithm..." Cooke disclosed an algorithm is used in finding the optimal solution, but failed to specify a predetermined parameter could be set when considering area and delay. However, Cooke has provided consideration to time and area in finding an optimal solution. Setting a predetermined parameter is an obvious manner in adjusting for a plurality of high level description language programs. Therefore, it would have been obvious.

Per claim 10:

-the depth of at least one branch in a group of connected nodes exceeds a predetermined threshold value, the thread divided in said first dividing step is defined as a block which is found out between two continuous memory accesses or I/0 accesses sharing the same I/0 port, or as an express machine introduced by a user, or as a branch connecting node of said control data flow graph.

Col. 6, line 22-29, "Each node in the task graph is assigned a priority. The priority is defined as the length of the longest path...A priority queue is initialized...", col. 6, lines 39-40, "All the load_configuration instructions may be issued at the beginning of the program if the total number of configurations...does not exceed the capacity...",col. 6, lines 53-59, "...block may still exceed the capacity..."

Cooke does traverse a branch of the graph of connected nodes and gives consideration to a threshold value (maximum capacity / area). Cooke disclosed dividing the threads. Cooke failed to disclose, "first dividing step is defined as a block which is found out between two continuous memory accesses or I/0 accesses sharing the same I/0 port, or as an express machine introduced by a user, or as a branch connecting node of said control data flow graph."

However, memory accesses, I/O accesses, an express machine introduces by a user or a branch are typical block constructs, and thus would have been obvious.

Per claim 11:

-said control step includes a loop having a memory access, said thread found out between the continuous 1/0 accesses is given with a loop extension dependency for determining whether or not a memory parallel exists in the iteration of said loop.

Col. 4, lines 29-31, "A single loop in the input source code may be transformed...into multiple constructs for runtime optimization and parallelization." Cooke failed to disclose "continuous 1/0 accesses is given with a loop extension dependency". Cooke gave consideration to loop constructs and parallelization in optimizing. Therefore it would have been obvious, to one of ordinary skill in the art, at the time of the invention to have modified Cooke's invention to include "thread found out between the continuous 1/0 accesses is given with a loop extension dependency for determining whether or not a memory parallel exists" because Cooke was optimizing loop parallelization, a well known optimization consideration.

Per claim 12:

-layout metrics for evaluating the area and the delay is used for the optimization in said second step.

Col. 4, lines 58-61, col. 5, lines 52-55.

Cooke disclosed area and time considerations when optimizing layout for circuits by analyzing high level description programs. Cooke failed to specifically disclose, "layout metrics for evaluating the area and the delay is used for the optimization in said second step". However, various steps would have been obvious to achieve the optimization of time and area when compiling a high level programming language, and thus it would have been obvious.

Per claim 16:

-said back-end compiler means carries out optimization by estimating a minimum boundary of an area and a waiting time in connection with any of a function unit, a register and a multiplexer. (See limitations as addressed in claim 2 above.)

Per claim 17:

-said back-end compiler means includes:

-a first dividing means for dividing the control data flow graph into threads composed of a set of the plurality of connected nodes and achieving the particular function;

-a first scheduling means of allocating a predetermined control step and a thread moving range in that step for a thread obtained in the first dividing means, the first scheduling means also allocating the order of priority for the threads respectively allocated with the control steps, in accordance with a plurality of priority order lists previously set;

-a first area restriction determining means for estimating a total area of the threads allocated in the first scheduling means, and for determining whether or not the estimated total area meets with the predetermined area restriction;

-when it is determined in the first area restriction determining means that the estimated total area does not meet with the predetermined area restriction, a similarity cost calculating means for calculating a similarity cost in connection with an area for all thread pair combinations of the threads obtained in the first dividing means;

-a first allocation means of selecting, from the thread pairs, a thread pair belonging to different control steps and having a further high similarity cost, with reference to the similarity costs obtained in the similarity cost calculating means, the first allocation means further obtaining a new thread by combining the selected thread pair as a new thread to another thread;

-a second area restriction determining means for estimating a total area for the new thread pair obtained in the first allocation means, and for determining whether or not the estimated total area meets with the predetermined area restriction;

-when it is determined in the second area restriction determining means that the estimated total area does not meet with the predetermined area restriction, an allocation-scheduling means for selecting, from the threads included in the list, a thread pair belonging to the same control step and having a further high similarity cost, in accordance with the plurality of priority order lists, in the order from a low priority list, the allocation-scheduling means obtaining a new thread pair by combining the selected thread pair as a new thread to another thread, and subdividing the control step allocated to the new thread pair, into two control steps having the same content;

-when it determined in the first or second area restriction determining means that the estimated total area meets with the predetermined area restriction, a thread processing means of investigating a trade-off between the area restriction and the waiting time restriction for the new thread pair obtained in the first allocation means or in the allocation-scheduling means, and carrying out the placement and routing of nodes to meet with both the restrictions;
-a second scheduling means for selecting and separating, for the threads placed and routed in the thread processing means, a thread pair having a low similarity, from the threads included in the list, in accordance with the plurality of priority order list, in the order from a high priority list;
-a second dividing means for assembling the thread pairs separated in the second scheduling means, into a context or a circuit which minimizes a connecting restriction between threads.
(See limitations as addressed in claim 5 above.)

Per claim 18:

-the predetermined time restriction includes three restrictions, a movement range restriction defined as a movement range of the thread in said control step, a thread sharing restriction defined as an overlapping in time between the threads in said control step, and a pipeline restriction defined as a waiting time for the thread belonging to one loop of a pipeline processing executing said control step in parallel.
(See limitations as addressed in claim 6 above.)

Per claim 19:

-said thread processing means carries out the placement and routing of said nodes, by

connecting a library supplying a set of function units which have a predetermined area and a predetermined delay and which have a predetermined parameter which can be set.

(See limitations as addressed in claim 9 above.)

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Steelman, whose telephone number is (703) 305-4564. The examiner can normally be reached Monday through Thursday, from 7:00 AM to 5:30 PM If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on (703) 305-4552. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mary Steelman

08/19/2004

ANTONY NGUYEN-BA
PRIMARY EXAMINER